## REMARKS

Applicants would like to thank the Examiner for the telephonic interview on August 25, 2004. The following remarks are made in response to an Interview Summary dated August 25, 2004. During the interview, the claims and art mentioned in the Interview Summary were discussed as described in the Interview Summary. Claims 1, 3, 5, 6, 8-10, 12-14, and 18-22 are hereby amended. Upon entry of the present Amendment, claims 1-22 are pending and presented for reconsideration.

**Summary of Support For Claim Amendments**

Support for the amendments to claims 1, 3, 5, 6, 8-10, 12-14, and 18-22 may be found in the Specification in, for example, paragraph [0007] on page 3, paragraph [0047] on page 15, paragraph [0051] on page 17, paragraph [0066] on page 23, and in paragraph [0076] on page 27. Applicants respectfully submit that no new matter has been added.

**Rejections of Claims 1-22 Under 35 U.S.C. §112, First Paragraph**

Claims 1-22 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

**Use of The Word "Instruction" In Claims**

The Office Action states that the Applicants' use the word "instruction" in claims 1-22 to refer to the data that is compared, and then suggests that "there is strong evidence that the word is either being used contrary to the Applicant's intent or in a manner contrary to common understanding." (Page 3). The Office Action specifically suggests (a) that it is unclear if the word "instruction" refers to something that a CPU executes or generates, citing paragraphs [0004] and [0006] of the Specification; (b) that "[c]omparing instructions prior to execution" to ensure that they are substantially identical does not put CPUs in failover mode, citing paragraph [0029]; and (c) that "'instructions' are actually the output of the CPUs," citing paragraph [0044].

Although Applicants believe that one of ordinary skill in the art at the time of filing of the application would understand Applicants' use of the word "instruction", Applicants have amended claims 1, 6, 8-10, 13-14, and 18-22 to change the word "instruction" to the word "output". No new matter has been added thereby. Applicants request reconsideration and withdrawal of the rejection of claims 1-22 under the first paragraph of 35 U.S.C. §112 because of the foregoing reasons.

**Rejections Under 35 U.S.C. §102**

Claims 1-10, 12-14, and 16-22 were rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent No. 6,141,769 to Petivan et al.

**Petivan**

Generally, Petivan teaches a fault tolerant computer system that includes "a first system module with a first processor and a first processor bus and a first I/O bus; a second system module with a second processor and a second processor bus and a second I/O bus; [and] a third system module with a third processor and a third processor bus and a third I/O bus." (Abstract). Petivan also teaches that each module includes a control device and comparison logic. (Abstract).

In Petivan's system, I/O controllers operate independently of each other and are not synchronized:

> [T]he I/O controllers of the TMR computer system operate independently of each other. They are not synchronized. That is, different operations may be initiated during the same time interval on the three I/O buses."

(Col. 4, lines 50-59).

**Rejection of Independent Claim 1 Under §102 In View of Petivan**

The Office Action suggests that Petivan anticipates all of the elements of amended claim 1.

Claim 1, as currently amended, is a fault-tolerant server comprising:

(a) a communications link comprising a switching fabric, a first communications channel, and a second communications channel;
(b) a first computing element in electrical communication with the communications link, the first computing element providing a first output to the communications link;
(c) a second computing element in electrical communication with the communications link, the second computing element providing a second output to the communications link;
(d) a first local input-output (I/O) module in electrical communication with the first computing element and the communications link; and
(e) a second local I/O module in electrical communication with the second computing element and the communications link,

wherein at least one of the first local I/O module and the second local I/O module compares the first output and the second output and indicates a fault of at least one of the first computing element and the second computing element upon the detection of a miscompare of the first output and the second output, and

wherein the first local I/O module is in electrical communication with the second local I/O module via a sync bus to synchronize the first local I/O module and the second local I/O module, the synchronization of the first local I/O module and the second local I/O module providing a verification of state information about the first computing element and the second computing element.

Claim 1 has been amended to recite "a first local input-output (I/O) module . . . ; and second local I/O module . . . , wherein the first local I/O module is in electrical communication with the second local I/O module via a sync bus to synchronize the first local I/O module and the second local I/O module, the synchronization of the first local I/O module and the second local I/O module providing a verification of state information about the first computing element and the second computing element." As an example, the state information of a computing element may include if the computing element is an "on-line" computing element (i.e. operating correctly), a "broken" computing element (i.e. operating incorrectly), or an "offline" computing element (i.e. executing diagnostics or ready to be brought into service).

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest that "[a] first local I/O module . . . in electrical communication with [a] second local I/O module via a sync bus to synchronize the first local I/O module and the second local I/O module, the synchronization of the first local I/O module and

the second local I/O module providing a verification of state information about the first computing element and the second computing element," as recited in amended claim 1. Thus, Petivan does not teach or suggest all of the elements of independent claim 1 as currently amended.

**Rejection of Independent Claim 13 Under §102 In View of Petivan**

The Office Action suggests that Petivan anticipates all of the elements of amended claim 13.

Claim 13, as currently amended, is a method for a first computing element and a second computing element to execute in lockstep in a fault-tolerant server comprising:

(a) establishing communication between the first computing element and a communications link, the communications link comprising a switching fabric, a first communications channel, and a second communications channel;
(b) establishing communication between the second computing element and the communications link;
(c) transmitting, by the first computing element, a first output to the communications link;
(d) transmitting, by the second computing element, a second output to the communications link; and
(e) comparing, by at least one of a local input-output (I/O) module of the first computing element and a local I/O module of the second computing element, the first output and the second output and indicating a fault of at least one of the first computing element and the second computing element in response thereto,
wherein the local I/O module of the first computing element is in electrical communication with the local I/O module of the second computing element via a sync bus to enable synchronization of the local I/O modules, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element.

Claim 13 has been amended to recite "[a] local I/O module of the first computing element is in electrical communication with [a] local I/O module of the second computing element via a sync bus to enable synchronization of the local I/O modules, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element." As an example, the state information of a computing element may include if the computing element is an "on-line" computing element (i.e. operating correctly), a

"broken" computing element (i.e. operating incorrectly), or an "offline" computing element (i.e. executing diagnostics or ready to be brought into service).

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest that "the local I/O module of the first computing element is in electrical communication with the local I/O module of the second computing element via a sync bus to enable synchronization of the local I/O modules, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element, " as recited in amended claim 13. Thus, Petivan does not teach or suggest all of the elements of independent claim 13 as currently amended.

**Rejection of Independent Claim 22 Under §102 In View of Petivan**

The Office Action suggests that amended claim 22 is unpatentable in view of Petivan.

Claim 22, as currently amended, is an apparatus for enabling a first computing element and a second computing element to execute in lockstep in a fault-tolerant server comprising:

(a) means for establishing communication between the first computing element and a communications link, the communications link comprising a switching fabric, a first communications channel, and a second communications channel;
(b) means for establishing communication between the second computing element and the communications link;
(c) means for transmitting, by the first computing element, a first output to the communications link;
(d) means for transmitting, by the second computing element, a second output to the communications link;
(e) means for comparing, by at least one of a local input-output (I/O) module of the first computing element and a local I/O module of the second computing element, the first output and the second output and indicating a fault of at least one of the first computing element and the second computing element in response thereto; and
(d) means for synchronizing the local I/O module of the first computing element and the local I/O module of the second computing element, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element.

Claim 22 has been amended to recite "means for synchronizing the local I/O module of the first computing element and the local I/O module of the second computing element, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element." As an example, the state information of a computing element may include if the computing element is an "on-line" computing element (i.e. operating correctly), a "broken" computing element (i.e. operating incorrectly), or an "offline" computing element (i.e. executing diagnostics or ready to be brought into service).

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest "means for synchronizing the local I/O module of the first computing element and the local I/O module of the second computing element, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element," as recited in amended claim 22. Thus, Petivan does not teach or suggest all of the elements of independent claim 22 as currently amended.

**Rejection of Dependent Claims Under §102 In View of Petivan**

Applicants respectfully submit that claims 2-10, 12, 14, and 16-21 are patentable because they depend on patentable independent claims (amended claims 1 and 13, respectively) as described above.

Therefore, in light of the foregoing reasons, Applicants respectfully request that the rejections under 35 U.S.C. §102 based on Petivan be reconsidered and withdrawn.

**Rejections Under 35 U.S.C. §103**

The Office Action rejects claims 11 and 15 under 35 U.S.C. §103(a) as being unpatentable over Petivan as applied to claims 1 and 13. In particular, with respect to claim 11, the Examiner takes official notice of a 1U rack-mount form factor circuitry, such as a

motherboard. In particular, with respect to claim 15, the Examiner takes official notice of error detection and correction in communications, examples of which are CRC, ECC, and parity.

Because Petivan's I/O controllers operate independently of each other and are not synchronized, Petivan does not teach or suggest that "[a] first local I/O module . . . in electrical communication with [a] second local I/O module via a sync bus to synchronize the first local I/O module and the second local I/O module, the synchronization of the first local I/O module and the second local I/O module providing a verification of state information about the first computing element and the second computing element" as recited in amended claim 1. Similarly, Petivan does not teach or suggest that "the local I/O module of the first computing element is in electrical communication with the local I/O module of the second computing element via a sync bus to enable synchronization of the local I/O modules, the synchronization of the local I/O modules providing a verification of state information about the first computing element and the second computing element" as recited in amended claim 13. Thus, Applicants respectfully submit that claims 11 and 15 are patentable because they depend on patentable independent claims (amended claims 1 and 13, respectively).

Therefore, in light of the foregoing reasons, Applicants respectfully request that the rejections under 35 U.S.C. §103 be reconsidered and withdrawn.

## SUMMARY

Claims 1-22 were pending in the Application. Applicants request that the Examiner reconsider the application and claims 1-22 in light of the foregoing Amendment and Response, and respectfully submit that the claims are in condition for allowance.

If, in the Examiner's opinion, a telephonic interview would expedite the favorable prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,

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